5 WATT HIGH EFFICIENCY WIDEBAND 7 TO 11 GHZ HBT MMIC POWER AMPLIFIER

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ABSTRACT

A fully monolithic HBT power amplifier that has established new benchmarks for bandwidth and efficiency at X-band is reported. Power-added efficiencies of 56% max/38% min/44.4% average across 7 to 11 GHz are the highest X-band efficiencies and widest bandwidth reported for MMIC HPA's. These amplifiers have demonstrated high power levels (up to 7.3 Watts) with high gain (11 to 14.1 dB) under thermally challenging long pulse (500 μsec) high duty cycle (25%) conditions. The amplifiers were fabricated using an advanced re-aligned AlGaAs/GaAs power HBT process with a plated bathtub heat sink.

INTRODUCTION

Heterojunction Bipolar Transistors have continued to demonstrate their abilities as high power high efficiency microwave amplifiers [1,2,3]. HBTs offer conclusive advantages over other solid state devices in terms of power density, operating voltage, and linearity. Reports of high performance AlGaAs/GaAs HBT's for microwave power applications however, often employ self-aligned technology in device fabrication which relies on complicated process steps. Although reduction of parasitic elements in the HBT structure is essential for high performance, uniformity of device charateristics and high yield are also critical. In this paper we will report on a new benchmark broadband 7 to 11 GHz MMIC HPA fabricated with a straightforward process using a re-aligned approach. E-beam lithography is utilized to obtain precise registration allowing reduction in emitter-base spacing. A thin emitter mesa ledge structure is created naturally during the base recess etching to reduce recombination and improve reliability. A thinned substrate with a flipside bathtub 25 μm underneath the active device cells and a selective plated heatsink of 10 μm thickness reduce the thermal resistance of the active device cells, greatly enhancing the microwave power performance and thermal stability of the amplifier. The epitaxial layers are grown using OMVPE, with Carbon as the base layer dopant for reliable operation under high current bias. Further details of this high yield/high performance process including epitaxial layer structure have been published previously [4,5].

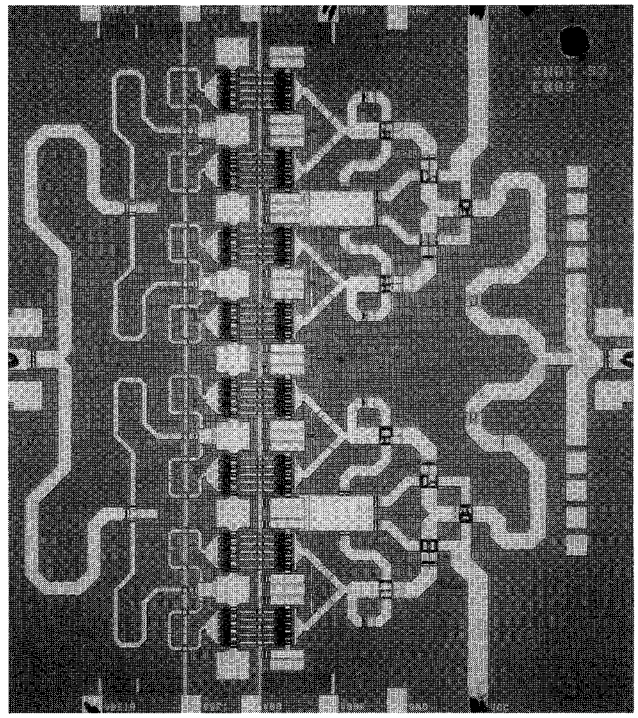

Figure 1: 5 Watt High Efficiency Fully Monolithic 7 to 11 GHz HBT Power Amplifier (3.0 mm x 3.4 mm)

CIRCUIT CONFIGURATIONS

Heterojunction Bipolar Transistor amplifiers published to date, have been operated in three configurations of the amplifying device: common emitter, common base, and cascode, a compound transistor wherein a common emitter drives a common base directly. We believe the cascode offers the best

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combination of attributes for high gain, highly efficient wideband amplification. The connection of the individual HBT sub-cells to form the compound cascode transistor yields the gain of a two-stage design in the area occupied by a single-stage amplifier. The common emitter stage provides the current gain, while the common base stage provides the voltage gain. Furthermore, the common emitter stage is operated at a low V_{ce}, increasing F_T and thus gain, while the common base operates at a high V_{ce}, maximizing power output and efficiency. Unlike the common emitter configuration, the feedback capacitance C_{bc} no longer appears from output to input. Similarly, the low input impedance of the common base configuration makes the matching problem severe. The input impedance of the cascode is higher than either due to enhanced unilaterality, and thus wideband impedance matching is easier.

CIRCUIT DESIGN

The design of this power amplifier is based upon a comprehensive methodology that includes both measurements and linear/non-linear modeling. De-embedded small signal S-parameters of the device cell are measured and equivalent circuit models are fitted to the data. Small signal models were created at both V_{ce} = 3.5 Volts and V_{ce} = 7.5 Volts with a collector current of I_c = 0.2 mA/μm², corresponding to the quiescent class AB operating condition of the two devices in the cascode connection. Load pull data is then employed to derive a parallel RC equivalent of the optimum power class B load impedance. In this case, R_{opt} = 53.4 ohms and C_{opt} = 0.2256 pF was utilized per 300 μm² cell. Considerable effort was also placed in obtaining a consistent set of coefficients for a non-linear model. Parameters are initially derived using small-signal models and I/V measurements. The coefficients are then least square optimized so that the non-linear model accurately predicts discrete device measured power performance from 1 dB compression into saturation (P_{out} and PAE vs P_{in}). The measured load-pull data and both the linear and non-linear models are then employed in the analysis and optimization of the design.

The design of a cascode MMIC HBT power amplifier can be segmented into the synthesis, analysis, and optimization of two matching networks, the input and output. The first step is to synthesize the output network which will transform 50 ohms to the required optimum large-signal power load impedance. The input networks are then designed to flatten small-signal gain and improve input impedance match. Subsequently, the designs are analyzed using harmonic balance and the Gummel-Poon model.

HBT AMPLIFIER DESCRIPTION

The device sub-cell geometry utilized is 2 emitter fingers of 1.5 μm by 20 μm dimensions with five sub-cells at 36 μm center-to-center separation per 300 μm² cell. A single base finger is utilized to reduce C_{bc} and improve gain. The amplifier, shown in Figure 1, consists of eight 300 μm² cells of each configuration (CE/CB), with quasi-lumped Chebyshev lowpass/bandpass structures used for impedance transformation. Total HBT periphery is 2400 μm² of common emitter (CE) and 2400 μm² of common base (CB). The design is fully monolithic, RF-testable on wafer, incorporates integral bias networks on chip (DC blocking capacitors and base bias current provided with collector to base feedback resistors), requires no external components, and a single V_{cc} supply for operation.

SIMULATED & MEASURED PERFORMANCE

The amplifiers were tested after die attach to a Au-plated CTE-matched carrier using Indium Lead solder. Figure 2 compares simulated small-signal input return loss and measured large-signal input return loss on one of the amplifiers. The close correlation between the two curves confirms that the HBT cascode input impedance is relatively constant from small-signal to saturation and validates the technique of using small-signal models for input network design. Figures 3 and 4 compare simulated and measured power output and power-added efficiency versus power input at a frequency of 8 GHz with good correlation between model and measurement. Measured power output, power-added efficiency, and power gain versus frequency of the MMIC power amplifier is shown in Figures 5 through 7. Data on three samples is depicted under test conditions of a 500 μsec pulse width at a 25% duty cycle. The power output over frequency of the samples is 5.44 Watts average, a maximum of 7.3 Watts, with 11 to 14.1 dB of power gain. Power-added efficiencies of 56% max/38% min/44.4% average across 7 to 11 GHz are the highest X-band efficiencies and widest bandwidth reported for MMIC HPA's in HBT[1], PHEMT[6], HFET[7], and MESFET[8] technologies.

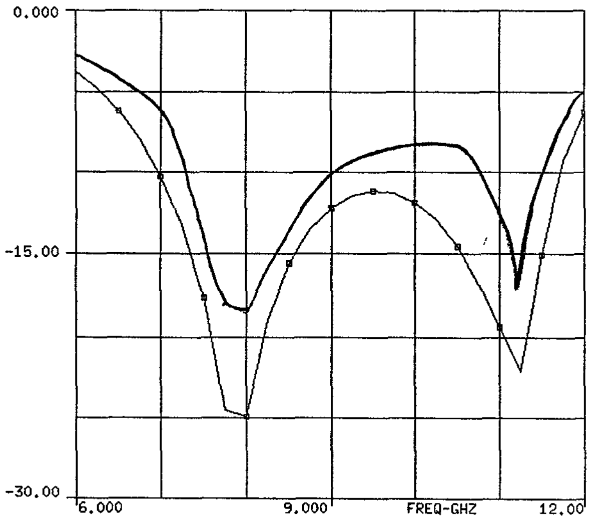

Figure 2: Simulated Small-Signal (lower curve) and Measured Large-Signal Input Return Loss (upper curve) of the HBT Power Amplifier

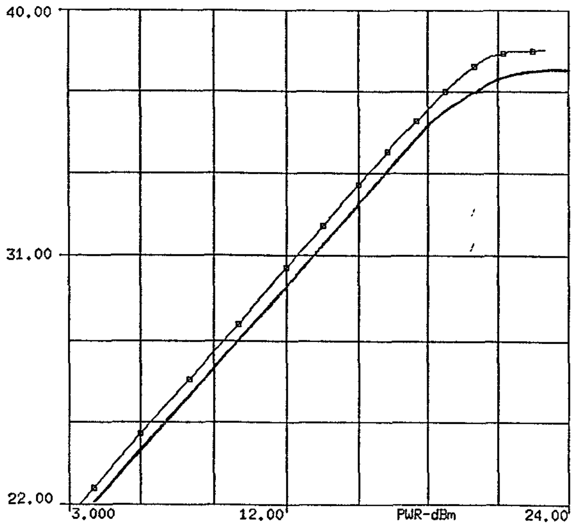

Figure 3: Simulated (upper curve) and Measured (lower curve) Power Output versus Power Input of the HBT Power Amplifier at 8 GHz

Power density figures of merit are likewise excellent. With 1.6 mm x 1.5 μm common base output periphery, 2.6 to 4.6 W/mm and 1.7 to 3.1 mW/μm² is achieved at the transistor level. The compact nature of the cascode is evident in the 0.4 to 0.7 Watts/mm² of GaAs area. This significant size advantage compared to other solid state technologies translates into reduced cost.

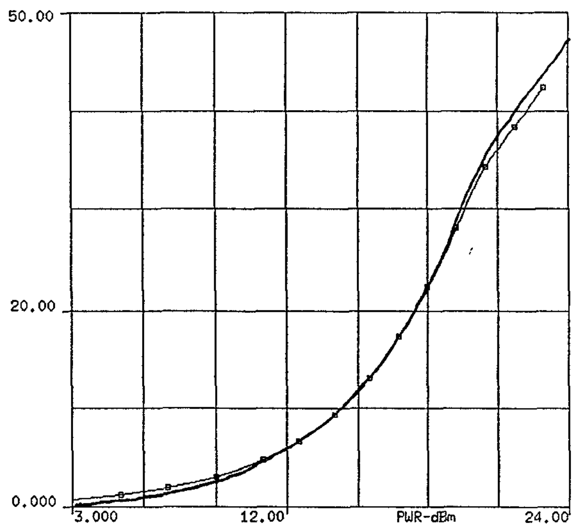

Figure 4: Simulated and Measured Power-Added Efficiency versus Power Input of the HBT Power Amplifier at 8 GHz

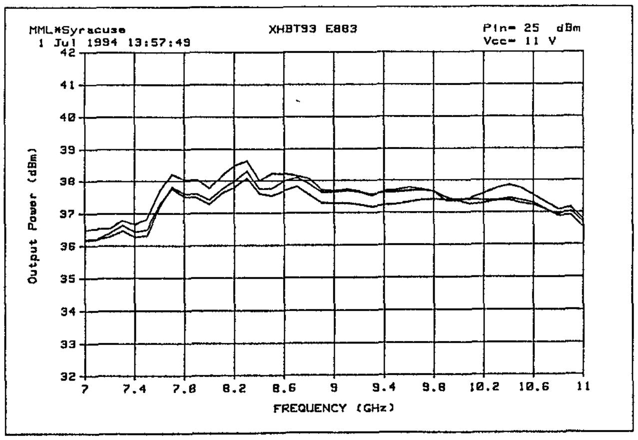

Figure 5: Power Output versus Frequency (3 Samples of the HPA)

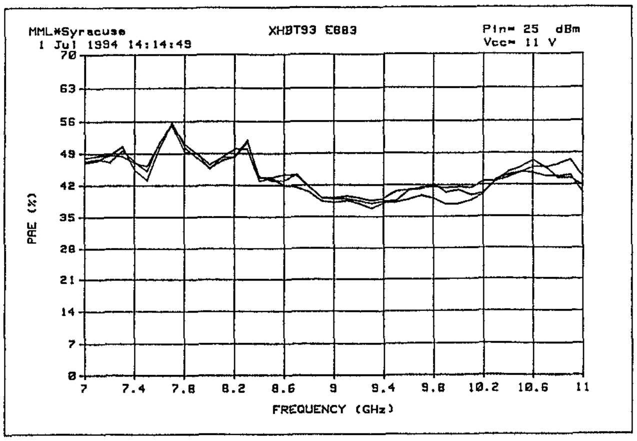

Figure 6: Power-Added Efficiency versus Frequency (3 Samples of the HPA)

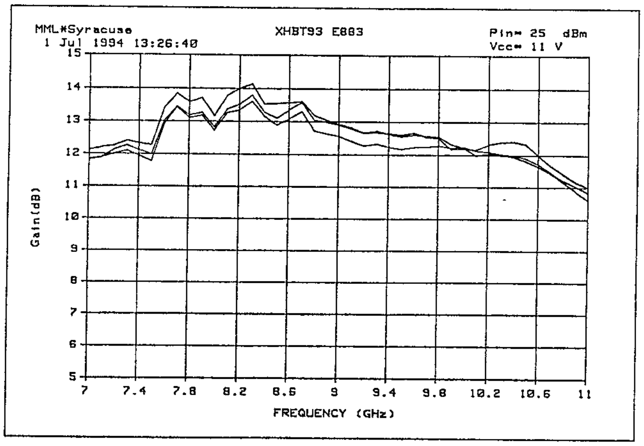

Figure 7: Power Gain versus Frequency (3 Samples of the HPA)

REFERENCES

[1] A. Khatibzadeh, W. Liu, T. Henderson, J. Sweder, S. Pierce, "High-Efficiency X-Band HBT Power Amplifier," 1994 IEEE Microwave and Millimeter-Wave Monolithic Circuits Symposium, May 22-25, 1994, San Diego, CA, pp 117-120.

[2] F. Ali, A. Gupta, M. Salib, B. Veasel, D. Dawson, "A 25 Ohm, 2W, 8-14 GHz HBT Power MMIC With 20 dB Gain and 40% Power Added Efficiency," 1994 IEEE Microwave and Millimeter-Wave Monolithic Circuits Symposium, May 22-25, 1994, San Diego, CA, pp 113-115.

[3] J. Komiak, L. Yang, "Highly Linear Efficient HBT MMIC Power Amplifiers," 1994 IEEE GaAs IC Symposium, October 16-19, 1994, Philadelphia, PA, pp 295-298.

[4] L. Yang, J. Komiak, M. Kao, D. Houston, D. Smith, K. Nordheden, "E-Beam Re-Aligned HBTs and A New Broadband MMIC Power Amplifier Using Bathtub as Heat Sink," 1994 IEEE International Electron Devices Meeting, December 11-14, 1994, San Francisco, CA, pp 203-206.

[5] L. Yang, J. Komiak, D. Smith, M. Kao, R. Brozovich, K. Nordheden, D. Helms, D. Houston, F. Bardsley, "Manufacturing Technology for High Performance HBT Linear Power Amplifiers," 1994 IEEE GaAs IC Symposium, October 16-19, 1994, Philadelphia, PA, pp 127-130.

[6] T. Apel, R. Bhatia, B. Lauterwasser, "High Performance Wide-Band & Medium-Band Power Amplifier MMICs," 1993 IEEE GaAs IC Symposium, October 10-13, 1993, San Jose, CA, pp 359-362.

[7] S. Cooper, K. Anderson, K. Salzman, R. Culbertson, J. Mason, D. Bryant, P. Saunier, "8 Watt High Efficiency X-Band Power Amplifier Using AlGaAs/GaAs HFET Technology," 1992 IEEE GaAs IC Symposium, October 4-7, 1992, Miami Beach, Florida, pp 183-185.

[8] H. Le, Y. Shih, V. Hwang, T. Chi. K. Kasel, D. Wang, "An X-Band High-Efficiency Ion-Implanted MMIC Power Amplifier," 1991 IEEE Microwave and Millimeter-Wave Monolithic Circuits Symposium, June 10-11, 1991, Boston, MA, pp 89-91.